Area-Dependent Photodetection Frequency Response Characterization of Silicon Avalanche Photodetectors Fabricated With Standard CMOS Technology

Myung-Jae Lee, *Student Member, IEEE*, and Woo-Young Choi, *Member, IEEE*

***Abstract*—We investigate the area-dependent characteristics of photodetection frequency responses of 850-nm silicon avalanche photodetectors (APDs) fabricated with standard complementary metal–oxide–semiconductor (CMOS) technology. CMOS-compatible APDs (CMOS-APDs) based on a p^+/n-well junction with four different device areas are used for the investigation, and we identify factors that influence photodetection frequency responses with the goal of achieving optimal photodetection bandwidth performance. Their current–voltage characteristics, electrical reflection coefficients, and photodetection frequency responses are measured, and the characteristics of the CMOS-APD photodetection frequency responses are analyzed using equivalent circuit models. From this, it is clarified how the four different factors of photogenerated-carrier transit time, device RC time constant, inductive-peaking effect, and parasitics contribute to the photodetection frequency responses and how their contribution changes with device areas. Among the four types of CMOS-APDs investigated in this study, the 10×10 μm^2 CMOS-APD has the largest 3-dB photodetection bandwidth of 7.6 GHz.**

***Index Terms*—Avalanche photodetector (APD), avalanche photodiode, equivalent circuit model, optical interconnect, optical receiver, photodetection bandwidth, photodetector, photodiode, silicon photonics, standard complementary metal–oxide–semiconductor (CMOS) technology.**

I. Introduction

With the data-rate requirement continuously increasing for many interconnect applications, fiber-optic technology is expanding its applications from long-distance communication applications into high-data-rate interconnect applications [1], [2]. For this, the development of cost-effective and compact optical devices is essential, and it can be of great advantage if such optical devices are compatible with existing silicon technology so that they can be monolithically integrated [1]–[3]. Recently, there have been rapidly growing research activities in the field of silicon photonics for achieving this goal [1]–[5].

Manuscript received October 2, 2012; revised December 19, 2012; accepted January 13, 2013. Date of publication February 12, 2013; date of current version February 20, 2013. This work was supported by the National Research Foundation of Korea funded by the Korean Government (MEST) under Grant 2012R1A2A1A01009233. The review of this paper was arranged by Editor S. Ralph.

The authors are with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea (e-mail: fodlmj@yonsei.ac.kr; wchoi@yonsei.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2013.2240684

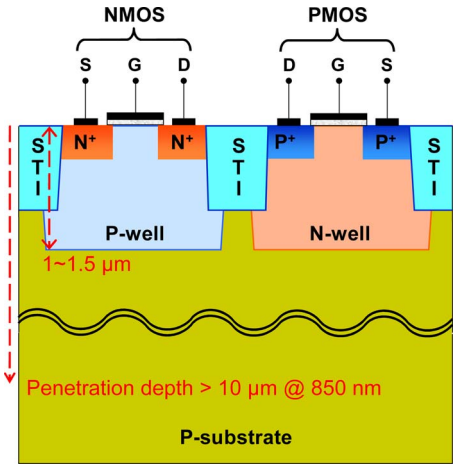


Fig. 1. Simplified cross section of typical twin-well CMOS transistors.

Although most works in silicon photonics are based on 1550-nm wavelength, using silicon as the photodetection material for 850-nm wavelength is also an interesting approach as it allows fabrication of photodetectors using standard silicon complementary metal–oxide–semiconductor (CMOS) technology without any process modification as well as very straightforward realization of monolithically integrated silicon optical receivers. The fact that there exists a significant demand for short-distance optical interconnect systems based on 850-nm vertical-cavity surface-emitting lasers and multimode fiber justifies this approach [6], [7].

However, there are inherent limitations of standard CMOS technology for photodetector applications. Fig. 1 shows the simplified cross section of typical twin-well CMOS transistors. With these, p-n junctions necessary for photodetectors can be realized with n-well/p-substrate, n^+/p-well, or p^+/n-well junctions. These p-n junctions are, however, formed within about 1.5 μm below the silicon surface, and their depletion lengths are not large enough to completely absorb 850-nm light, which has optical penetration depth over 10 μm in silicon [7]. The 850-nm light penetrates deep into the silicon substrate, resulting in reduction of responsivity due to recombination of photogenerated carriers in charge-neutral regions. Furthermore, those photogenerated carriers contributing to photocurrents have to diffuse through charge-neutral regions, which significantly limit the photodetection frequency response.

We have previously reported high-performance CMOS-compatible avalanche photodetectors (APDs) (CMOS-APDs)

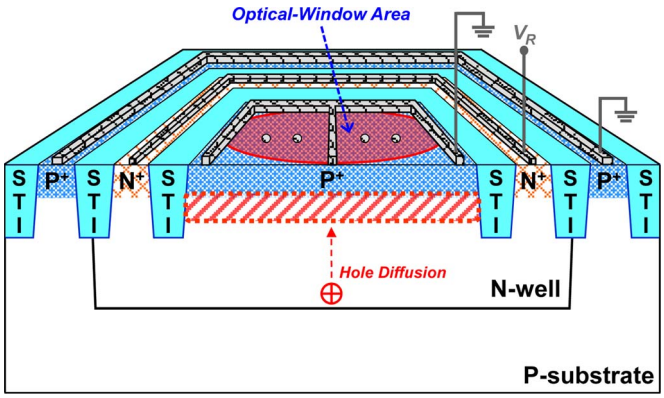


Fig. 2. Structure of the fabricated CMOS-APDs.

which overcome the aforementioned problems [8]–[11]. Specifically, our CMOS-APDs are based on a p^+/n-well or an n^+/p-well junction, which provides higher photodetection bandwidth without slow photogenerated diffusion currents in the p-substrate region. In addition, photodetection responsivity can be greatly enhanced by large avalanche gain.

In this paper, we investigate the area-dependent photodetection frequency responses of CMOS-APDs for the goals of identifying the factors that influence the photodetection bandwidth and achieving an optimal photodetection bandwidth. p^+/n-well CMOS-APDs having four different device areas are realized, and their current–voltage characteristics, electrical reflection coefficients, and photodetection frequency responses are measured. Then, an equivalent circuit model is developed for each type of CMOS-APD from the measurement results. The resulting equivalent circuits are then analyzed for understanding the CMOS-APD photodetection frequency response. From this investigation, dominant factors that influence the photodetection frequency responses are identified, and their influences are clarified for different device areas. Among the investigated devices, the CMOS-APD having the 10×10 μm^2 device area is found to have the largest 3-dB photodetection bandwidth of 7.6 GHz, which we believe is the largest value reported for 850-nm photodetectors fabricated with standard CMOS technology.

This paper is organized as follows. Section II describes the structures of the CMOS-APDs used in our investigation as well as the results of their characteristic measurements. Section III gives the equivalent circuit models for CMOS-APDs and the analyses of the photodetection frequency responses using the models. Section IV summarizes this paper.

II. Device Structures and Measurement Results

Fig. 2 shows the basic structure of CMOS-APDs used in our investigation. They are based on a p^+/n-well junction fabricated with 0.13-μm standard CMOS technology having one poly and seven metals. Four types of CMOS-APDs having optical-window areas of 10×10, 20×20, 30×30, and 40×40 μm^2 are realized. Shallow trench isolation (STI), used in standard CMOS technology for device isolation, is inserted as a guard ring between the p^+ and n^+ regions since it provides

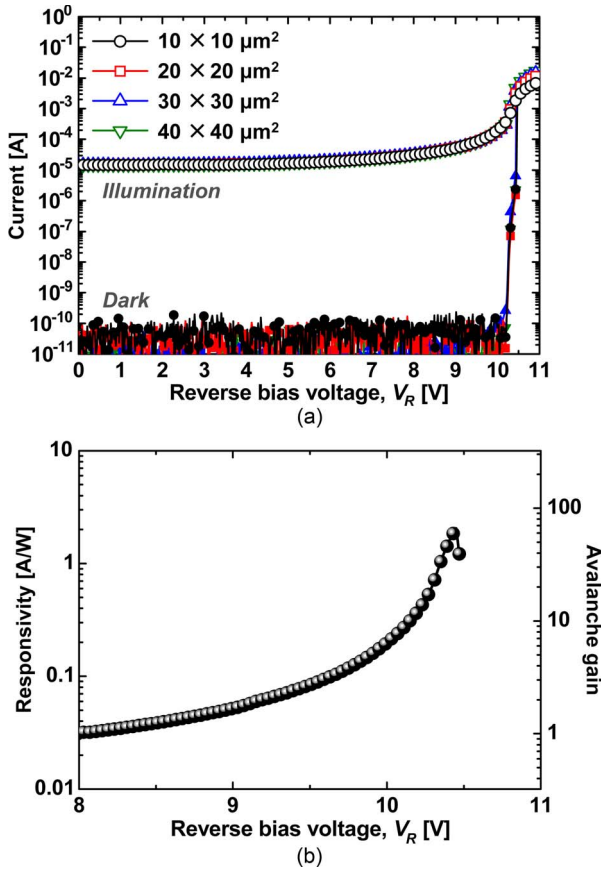


Fig. 3. (a) Current–voltage characteristics of CMOS-APDs and (b) responsivity and avalanche gain of the 10×10 μm^2 CMOS-APD as functions of reverse bias voltage.

a high uniform electric field profile without premature edge breakdown, resulting in high responsivity [10]. For optical-window formation, the salicide process is blocked. Multifinger electrodes of 0.2 μm wide are formed for p^+ contacts located in the n-well region. All CMOS-APDs are fabricated without any design or layout rule violation. The p^+/n-well junction is reverse biased with a positive voltage applied to the n-well contacts, and p^+ is grounded. The p-substrate contacts are also grounded. In order to eliminate the influence of slow diffusion currents generated in the p-substrate, we extract photocurrents from the electrode for the p^+ region within the n-well. As a result, slow diffusion currents due to absorption in the substrate do not contribute to the measured photocurrents.

Fig. 3(a) shows the current–voltage characteristics of the CMOS-APDs under illumination and dark conditions. For the measurements, light from an 850-nm laser diode was injected into the device using a lensed fiber having a 10-μm spot diameter. The optical power was 1 mW measured at the end of the lensed fiber. All the CMOS-APDs exhibit low dark currents below a few nanoamperes before avalanche breakdown. The CMOS-APDs having different device areas show similar current–voltage characteristics under the illumination condition. As the reverse bias voltage approaches the avalanche breakdown voltage of about 10.45 V, currents start to increase abruptly due to avalanche gain. The responsivity is only about 0.015 A/W at a reverse bias voltage of 1 V, but the maximum

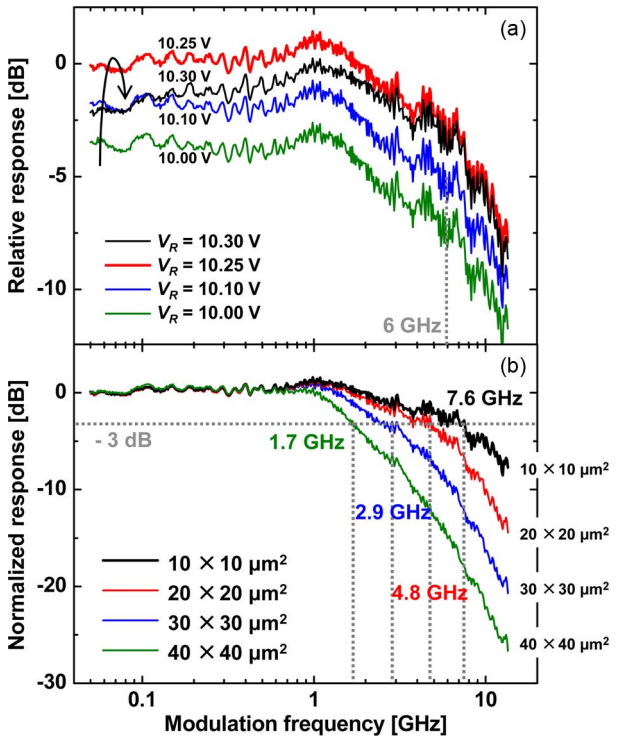
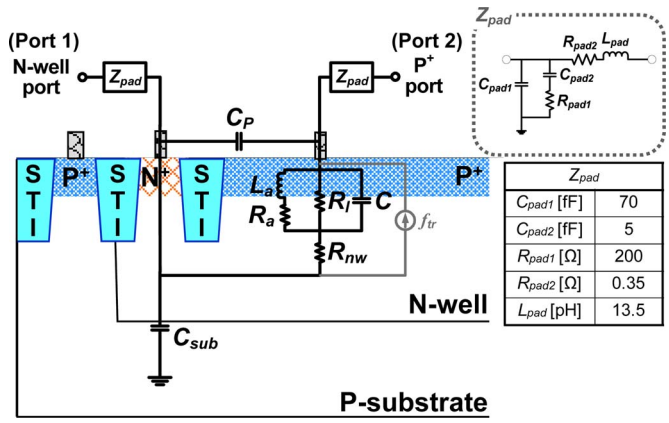


Fig. 4. (a) Photodetection frequency responses of the $10 \times 10\ \mu\text{m}^2$ CMOS-APD at different bias voltages. (b) Normalized photodetection frequency responses of CMOS-APDs having different device areas.

responsivity is about 2 A/W at the reverse bias voltage of 10.45 V, as shown in Fig. 3(b). When the reverse bias voltage is larger than the breakdown voltage, currents are saturated due to the series resistance and the space-charge effect [12]. Smaller devices saturate slightly earlier because they have higher parasitic resistance due to the smaller number of contacts and vias for the electrodes, but this difference is negligible at $V_R = 10.25$ V used in our investigation for optimal photodetection frequency response.

Fig. 4(a) shows the measured photodetection frequency responses of the $10 \times 10\ \mu\text{m}^2$ CMOS-APD at different bias voltages. For the measurements, an electrooptic modulator driven by a vector network analyzer (VNA) was used to modulate the light from an 850-nm laser diode. For all the frequency response measurements, the incident optical power had an average of 1 mW measured at the end of the lensed fiber. As the reverse bias voltage increases, the photodetection frequency response initially increases due to the increased avalanche gain. However, if the bias voltage is too large, the low frequency response starts to decrease, as can be seen in Fig. 4(a). For the application that we have in mind, this is not a desirable effect, and consequently, we determine the bias voltage of 10.25 V as the optimal condition for our investigation. The CMOS-APDs with different device areas show similar dependence on the bias voltage.

Fig. 4(b) shows the photodetection frequency responses for CMOS-APDs having four different areas measured at the optimal bias voltage of 10.25 V. As can be seen in the figure, smaller devices have larger photodetection bandwidth, reaching 7.6 GHz for the $10 \times 10\ \mu\text{m}^2$ CMOS-APD.



Z_{pad}	
C_{pad1} [fF]	70
C_{pad2} [fF]	5
R_{pad1} [Ω]	200
R_{pad2} [Ω]	0.35
L_{pad} [pH]	13.5

Fig. 5. Equivalent circuit model for CMOS-APDs.

III. Analyses With Equivalent Circuit Models

A. Equivalent Circuit Models for CMOS-APDs

To better understand CMOS-APD photodetection frequency response characteristics, we derived equivalent circuit models for CMOS-APDs. Fig. 5 shows the equivalent circuit model used for our investigation, which is a simplified version of that reported in [13]. An inductor with a series resistor, and a parallel resistor and a capacitor are used for modeling the APD core. The inductance L_a represents the phase delay between currents and voltages due to impact ionization [14]. The series resistance R_a accounts for the finite reverse saturation current and the field-dependent velocity [14]. R_l and C are the resistance and capacitance of the depletion region, respectively. R_{nw} and C_{sub} represent the n-well resistance and the n-well/p-substrate junction capacitance, respectively. C_p is the parasitic capacitance between the n^+ and p^+ electrodes, and Z_{pad} represents the equivalent circuit for pads and metal interconnects with details shown in the inset in Fig. 5.

The photodetection frequency response is also affected by the transit time of photogenerated carriers. For photodetectors fabricated with standard CMOS technology, this is dominated by diffusion of photogenerated carriers in charge-neutral regions, which, in our case, corresponds to hole diffusion in the charge-neutral n-well region as shown in Fig. 2. The influence of transit time is modeled in the equivalent circuit with a current source having a single-pole frequency response, where f_{tr} represents the 3-dB bandwidth limited by hole-diffusion transit time [15].

B. Parameter Extraction for Equivalent Circuits

The parameter values for the passive circuit elements in the equivalent circuit are extracted from two-port S-parameter measurements performed from 50 MHz to 13.5 GHz using a VNA under 1-mW optical illumination. On-wafer calibration is done prior to measurements. Advanced Design System (ADS) by Agilent Technologies is used for S-parameter extraction. First, Y-parameters and Z-parameters are calculated from the measured S-parameters, and open and short test patterns are used for extracting Z_{pad} parameters. The extracted parameters are listed in Fig. 5. Then, C_{sub} is extracted by Z_{12}, and the other parameters are extracted by $Z_{22} - Z_{12}$ through a fitting

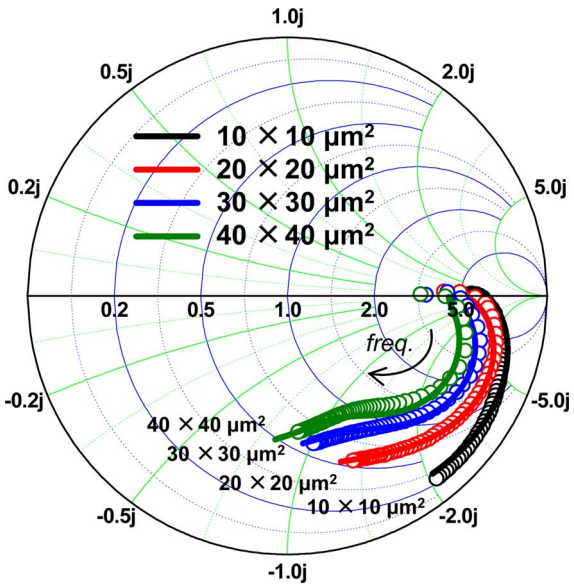


Fig. 6. Measured and simulated electrical reflection coefficients for different CMOS-APDs at the reverse bias voltage of 10.25 V. The hollow circles represent the measured data, and the solid lines represent the simulated results.

TABLE I
EXTRACTED PARAMETERS FOR CMOS-APDs ACCORDING TO DEVICE AREAS

	10×10 [μm²]	20×20 [μm²]	30×30 [μm²]	40×40 [μm²]
L_a [nH]	13			
R_a [Ω]	150			
R_l [kΩ]	1.2			
C [fF]	35	140	315	560
R_{nw} [Ω]	60	50	40	30
C_{sub} [fF]	15	45	90	150
C_p [fF]	20	60	120	180

process [13]. The frequency-dependent current source is not included during this extraction and fitting process since it does not influence the values of the passive circuit elements in the small-signal analysis. For fitting, initial guesses are made from theoretical equations and then manually refined [13]. Fig. 6 shows the electrical reflection coefficients at the p^+ port on the Smith chart from 50 MHz to 13.5 GHz for different CMOS-APDs biased at 10.25 V, from measurement and simulation with extracted parameter values. Table I shows the values for the extracted parameters that are used for the simulation. The extracted values for L_a, R_a, and R_l are the same for all device types. Avalanche inductor L_a does not change with the device area at the same bias condition since all CMOS-APDs have the same avalanche multiplication characteristics based on the same p^+/n-well junction and guard ring as shown in Fig. 3(a). R_a represents the series resistance associated with the avalanche inductor L_a and determines the avalanche inductor quality factor, which is not directly related to the device area [14]. R_l is defined as the voltage-to-current ratio in the vicinity of 0 V, and all CMOS-APDs have similar slope of the current–voltage curve as shown in Fig. 3(a), resulting in the same R_l for all device types. The junction capacitance C is proportional to the device area. $C_{\rm sub}$ and C_p also increase with the device area, but $R_{\rm nw}$ does not change very much because the increase in lateral resistance compensates the decrease in vertical resistance with larger devices.

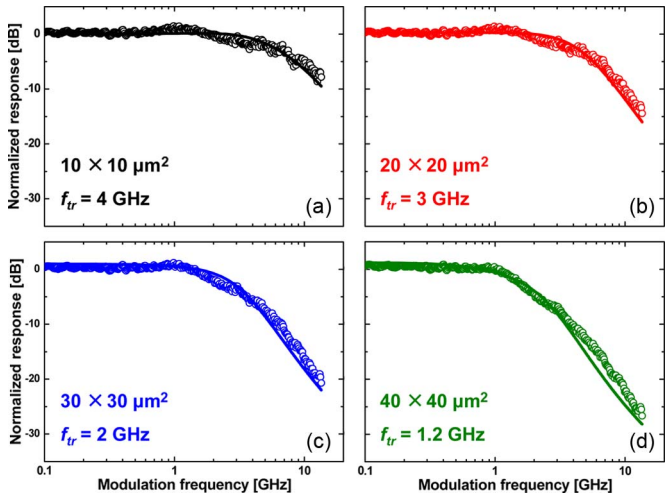


Fig. 7. Measured and simulated photodetection frequency responses for different CMOS-APDs at the reverse bias voltage of 10.25 V. The hollow circles represent the measured data, and the solid lines represent the simulated results.

Once the parameter values for the passive circuit elements are determined, the $f_{\rm tr}$ value for the frequency-dependent current source is determined by fitting the simulated photodetection frequency responses to measurement results. For the simulation, ADS is used. Fig. 7 shows the normalized measured and simulated photodetection frequency responses for CMOS-APDs having different device areas at the reverse bias voltage of 10.25 V. Also shown in each figure is the value of $f_{\rm tr}$ that gives the best fitting between measurement and simulation. The fitted $f_{\rm tr}$ value decreases as the device area increases due to the increase of the lateral diffusion path.

C. Analyses

The photodetection frequency response of an APD can be influenced by four different factors: transit time of photogenerated carriers, device RC time constant, inductive-peaking effect, and parasitics. In order to identify how each of these factors influences our CMOS-APDs, we perform analyses in which only certain factors among these four are considered at a time, and the resulting photodetection frequency responses are compared. This can be easily done by simulating the photodetection frequency response with an equivalent circuit in which certain circuit elements are intentionally left out.

Fig. 8 shows the simulated photodetection frequency responses of CMOS-APDs having different device areas at the reverse bias voltage of 10.25 V under various conditions. For each type of device, four different simulation results are shown: one that considers only the photogenerated-carrier transit time (not including L_a, R_a, R_l, C, $R_{\rm nw}$, $C_{\rm sub}$, and C_p), another that considers only the RC time constant (not including $f_{\rm tr}$ in the current source as well as L_a and R_a), third that considers the inductive-peaking effect (not including $f_{\rm tr}$ in the current source), and fourth that includes all the factors which are also shown in Fig. 7. In Fig. 8, it can be observed that the transit

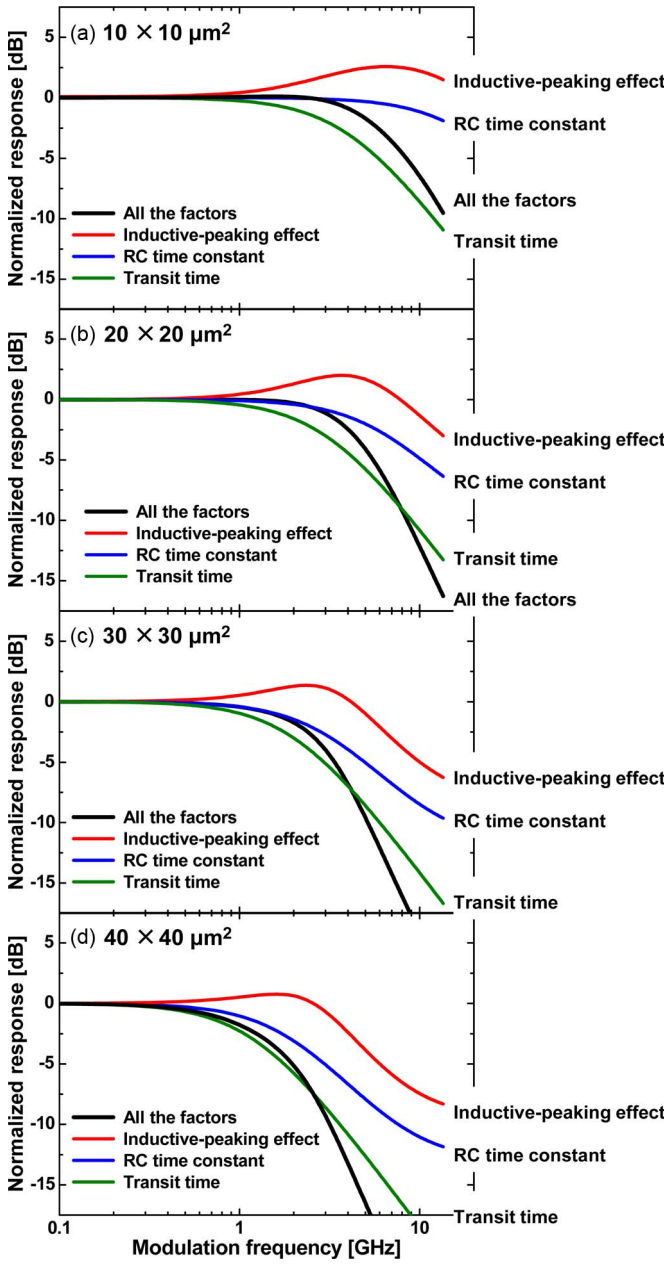


Fig. 8. Normalized photodetection frequency responses of CMOS-APDs for the photogenerated-carrier transit time, the RC time constant, the inductive-peaking effect, and all the factors according to device areas.

time is the dominant bandwidth-limiting factor. Even with this limitation, however, higher total bandwidth can be achieved because inductive peaking provides high-frequency boosting. The 10×10 μm^2 CMOS-APD has 7.6-GHz photodetection bandwidth with the inductive-peaking effect at 6.5 GHz while its $f_{\rm tr}$ is 4 GHz.

Fig. 9 compares the influence of each effect for devices with different device areas. Fig. 9(b) shows that smaller devices have higher inductive-peaking frequencies. This is because the capacitance becomes smaller with the decreasing device area and the inductive-peaking frequency is inversely proportional to the square root of capacitance. Fig. 9(c) and (d) shows that the photodetection frequency responses for the RC time constant and the transit time have larger bandwidth as the device

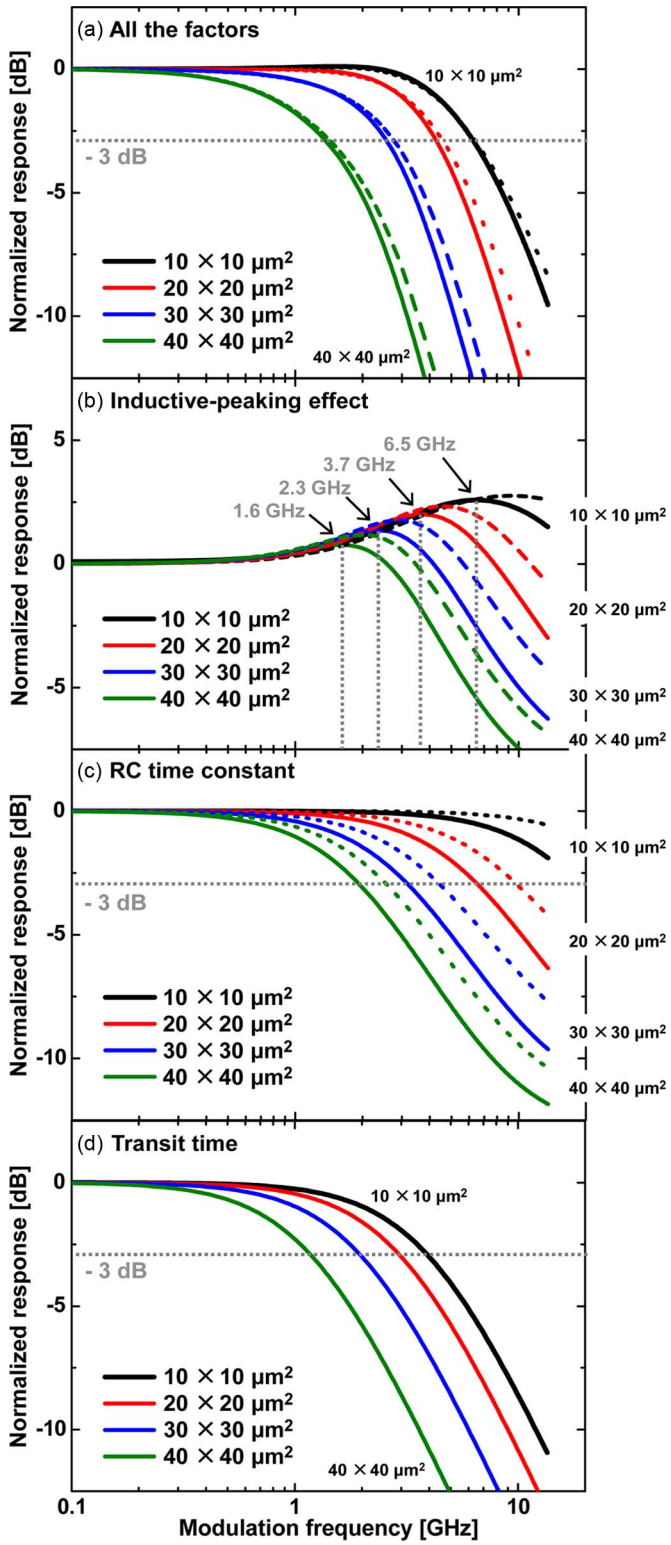


Fig. 9. Normalized photodetection frequency responses of CMOS-APDs having different device areas for (a) all the factors, (b) the inductive-peaking effect, (c) the RC time constant, and (d) the photogenerated-carrier transit time. The solid and dotted lines represent the simulated responses with and without the parasitics, respectively.

area decreases. This is due to the decrease in the capacitance for the RC time constant and the lateral diffusion path for the transit time. Fig. 9 also shows the simulated photodetection frequency responses with and without the parasitics. For

TABLE II
PERFORMANCE COMPARISON OF SILICON PHOTODETECTORS FABRICATED WITH STANDARD CMOS TECHNOLOGY

	[16]	[17]	[18]		This work	
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS	0.13-μm CMOS
Structure	Multiple p^+-p-n APD	$P^+/P^-/N^+$ lateral PIN	Strip SMPD*	Meshed SMPD*	P^+/N-well APD	P^+/N-well APD
R	0.74 A/W	0.073 A/W	0.057 A/W	0.029 A/W	0.48 A/W	0.48 A/W
BW	1.6 GHz	1.9 GHz	1.8 GHz	6.9 GHz	1.7 GHz	7.6 GHz
C_{PD}	345 fF	1600 fF	213 fF	206 fF	560 fF	35 fF
A	50×50 μm^2 (Square)	50×50 μm^2 (Square)	55×55 μm^2 (Octagon)	55×55 μm^2 (Octagon)	40×40 μm^2 (Square)	10×10 μm^2 (Square)
V_R	14.3 V	6 V	14.2 V	14.2 V	10.25 V	10.25 V

*SMPD: spatially modulated photodetector
R: responsivity, *BW*: bandwidth, C_{PD}: intrinsic photodetector capacitance, *A*: optical-window area, V_R: reverse bias voltage

simulation without the parasitics, $C_{\rm sub}$, C_p, and $Z_{\rm pad}$ are not included. Although the parasitics affect the photodetection frequency responses for the inductive-peaking effect and the RC time constant, they do not affect the total response very much as the limiting factor for our devices is the photogenerated-carrier transit time.

As a summary, the photodetection frequency response is limited by the transit time of holes photogenerated in the charge-neutral n-well region, but this is somewhat compensated by inductive peaking provided by the inductive component in the avalanche region. In addition, smaller devices have larger bandwidth because their hole transit time is smaller and the inductive-peaking frequency is higher with smaller capacitance.

The performances of various silicon photodetectors fabricated with standard CMOS technology are compared in Table II. Our 10×10 μm^2 CMOS-APD shows the best photodetection bandwidth performance of 7.6 GHz along with high responsivity.

IV. CONCLUSION

We have investigated the area-dependent characteristics of photodetection frequency responses of CMOS-APDs for the goals of identifying the factors that influence the photodetection bandwidth and, with it, achieving high-photodetection-bandwidth silicon photodetectors. Four types of CMOS-APDs having different device areas were realized, and their current–voltage characteristics, electrical reflection coefficients, and photodetection frequency responses were examined. From the measurement results, equivalent circuits were obtained. With simulation based on equivalent circuits, those factors that influence the photodetection frequency response have been investigated. It is determined that the photodetection bandwidth of our CMOS-APD is limited by the photogenerated-carrier transit time in the charge-neutral n-well region, but inductive peaking provides enhanced bandwidth. By reducing the device area up to 10×10 μm^2, the photodetection bandwidth of the CMOS-APD is enhanced to 7.6 GHz due to the decreased transit time and the higher inductive-peaking frequency. We believe that our CMOS-APDs are very useful for realizing high-speed 850-nm integrated optical receivers using the standard silicon technology.

ACKNOWLEDGMENT

The authors would like to thank IDEC for the EDA software support.

REFERENCES

[1] L. Pavesi and D. J. Lockwood, *Silicon Photonics*. Berlin, Germany: Springer-Verlag, 2004.
[2] B. Jalali and S. Fathpour, "Silicon photonics," *J. Lightw. Technol.*, vol. 24, no. 12, pp. 4600–4615, Dec. 2006.
[3] C. Gunn, "CMOS photonics for high-speed interconnects," *IEEE Micro*, vol. 26, no. 2, pp. 58–66, Mar./Apr. 2006.
[4] R. Soref, "The impact of silicon photonics," *IEICE Trans. Electron.*, vol. E91-C, no. 2, pp. 129–130, Feb. 2008.
[5] N. Izhaky, M. T. Morse, S. Koehl, O. Cohen, D. Rubin, A. Barkai, G. Sarid, R. Cohen, and M. J. Paniccia, "Development of CMOS-compatible integrated silicon photonics devices," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1688–1698, Nov./Dec. 2006.
[6] T. E. Sale, C. Chu, J.-K. Hwang, G.-H. Koh, R. Nabiev, J. L. Tan, L. M. Giovane, and M. V. R. Murty, "Manufacturability of 850 nm data communication VCSELs in high volume," in *Proc. SPIE—Vertical-Cavity Surface-Emitting Lasers XIV*, Feb. 2010, vol. 7615, pp. 761503-1–761503-10.
[7] T. K. Woodward and A. V. Krishnamoorthy, "1-Gb/s integrated optical detectors and receivers in commercial CMOS technologies," *IEEE J. Sel. Topics Quantum Electron.*, vol. 5, no. 2, pp. 146–156, Mar./Apr. 1999.
[8] H.-S. Kang, M.-J. Lee, and W.-Y. Choi, "Si avalanche photodetectors fabricated in standard complementary metal–oxide–semiconductor process," *Appl. Phys. Lett.*, vol. 90, no. 15, pp. 151118-1–151118-3, Apr. 2007.
[9] M.-J. Lee and W.-Y. Choi, "Performance comparison of two types of silicon avalanche photodetectors based on N-well/P-substrate and P^+/N-well junctions fabricated with standard CMOS technology," *J. Opt. Soc. Korea*, vol. 15, no. 1, pp. 1–3, Mar. 2011.
[10] M.-J. Lee, H. Rücker, and W.-Y. Choi, "Effects of guard-ring structures on the performance of silicon avalanche photodetectors fabricated with standard CMOS technology," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 80–82, Jan. 2012.
[11] M.-J. Lee and W.-Y. Choi, "A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain–bandwidth product," *Opt. Exp.*, vol. 18, no. 23, pp. 24 189–24 194, Nov. 2010.
[12] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007.
[13] M.-J. Lee, H.-S. Kang, and W.-Y. Choi, "Equivalent circuit model for Si avalanche photodetectors fabricated in standard CMOS process," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1115–1117, Oct. 2008.
[14] Y.-C. Wang, "Small-signal characteristics of a read diode under conditions of field-dependent velocity and finite reverse saturation current," *Solid State Electron.*, vol. 21, no. 4, pp. 609–615, Apr. 1978.
[15] G. Wang, T. Tokumitsu, I. Hanawa, K. Sato, and M. Kobayashi, "Analysis of high speed p-i-n photodiodes S-parameters by a novel small-signal equivalent circuit model," *IEEE Microw. Wireless Compon. Lett.*, vol. 12, no. 10, pp. 378–380, Oct. 2002.

[16] W.-K. Huang, Y.-C. Liu, and Y.-M. Hsin, "A high-speed and high-responsivity photodiode in standard CMOS technology," *IEEE Photon. Technol. Lett.*, vol. 19, no. 4, pp. 197–199, Feb. 2007.
[17] W.-Z. Chen and S.-H. Huang, "A 2.5 Gb/s CMOS fully integrated optical receiver with lateral PIN detector," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2007, pp. 293–296.
[18] S.-H. Huang, W.-Z. Chen, Y.-W. Chang, and Y.-T. Huang, "A 10-Gb/s OEIC with meshed spatially-modulated photo detector in 0.18- μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1158–1169, May 2011.

Myung-Jae Lee (S'08) received the B.S. and M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, Korea, in 2006 and 2008, respectively, where he is currently working toward the Ph.D. degree.

Woo-Young Choi (M'92) received the B.S., M.S., and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA, USA.

He is currently a Professor with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea.